

“Double Exposure Method”: a Novel Photolithographic Process to Fabricate Flexible Organic Field-Effect Transistors and Circuits

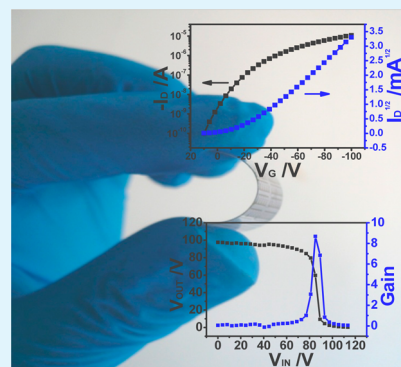
Deyang Ji, Lang Jiang,* Huanli Dong, Qing Meng, Zongrui Wang, Hantang Zhang, and Wenping Hu*

Beijing National Laboratory for Molecular Sciences, Key Laboratory of Organic Solids, Institute of Chemistry, Chinese Academy of Sciences, Beijing 100190, China

S Supporting Information

ABSTRACT: A novel process called “double exposure method” has for the first time been developed to utilize common organic materials as insulating layers at low annealing temperature in the process of photolithography. In this method, organic dielectric layer will not dissolve in the final lift-off step by using developer to replace traditional acetone. Bottom-gate bottom-contact (BGBC) OFETs are fabricated on the flexible PET substrates with polystyrene (PS) and pentacene as dielectric layer and semiconductor layer, respectively. Transistors with mobility of $0.36 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and logic inverter with gain of 9 on the plastic substrates have been fabricated, demonstrating the potential application of “double exposure method” in flexible organic electronics.

KEYWORDS: double exposure, polystyrene, flexible, OFETs, organic circuits



INTRODUCTION

Organic field-effect transistors (OFETs) and organic circuits as important branches of organic electronics have made breakthrough and shown great potential in flexible electronics in recent years.^{1–11} High integration and low-temperature processing of organic electronic devices is a promising tendency in the development of organic electronics toward practical applications. Therefore, it is urgent to develop effective high-resolution patterning techniques. As one of the most important patterning technologies, photolithography shows overwhelming advantages in reducing the minimal feature dimensions over other conventional printing techniques,^{12–14} with which high-resolution highly integrated OFETs and organic circuits could be fabricated.

Compared with conventional SiO_2 dielectric material, organic insulating materials are considered as ideal replacements because of their obvious advantages in fabricating flexible and low-cost electronic devices with high performance.^{15–20} However, a large proportion of organic insulating materials cannot endure conventional photolithographic processes (such as the influence of photoresist, development, and organic solvents in lift-off). Only a very few organic insulating materials (e.g., polyvinylphenol (PVP) mixed with special components^{15,16}) were reported to be processable in photolithography, but the high processing temperature (200 °C) and the high cost of materials limits its practical application in low-temperature low-cost flexible organic electronics. Meanwhile, although some other organic insulating materials (e.g., polystyrene (PS) and polymethyl methacrylate (PMMA)) have proven to be applicable in organic field-effect

transistors (OFETs)^{17–20} with low annealing temperature (~ 80 °C), they are easily damaged during the solution process of photolithography. To solve these problems and utilize the existing organic insulating materials at low annealing temperature, we developed a novel photolithographic method called “double exposure method” to eliminate the influence of developer over the soluble insulating materials. Polystyrene (PS), which possesses low annealing temperature (~ 80 °C) but high solubility, was chosen as a candidate of insulating materials to verify this “double exposure” photolithography. On the basis of this technique, OFETs and organic circuits on flexible substrates were successfully fabricated. This is the first time to retain PS as insulator layers in the process of photolithography. More significantly, “double exposure method” is also versatile to other organic insulator materials, such as polymethyl methacrylate (PMMA).

EXPERIMENTAL SECTION

The detailed procedure to manufacture OFETs by photolithography could be depicted as following: (i) $1 \mu\text{m}$ PS film was first prepared on polyethylene terephthalate (PET)/indium tin oxide (ITO) substrates by spin coating 80 mg/mL polystyrene

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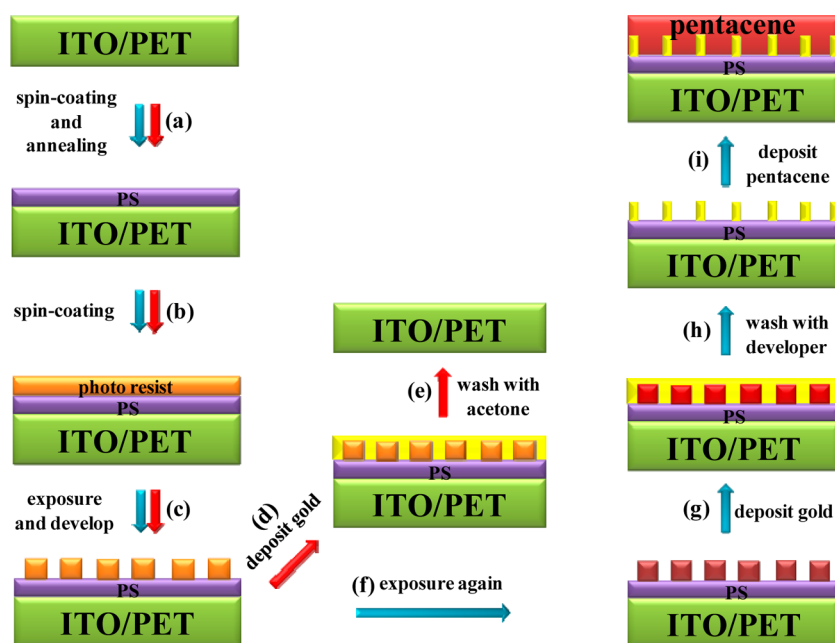


Figure 1. Schematic diagram of traditional photolithography and “double exposure method” to fabricate OFETs.

(PS) in toluene at 2000 r/min for 60 s, and then smooth film surface was obtained after annealing at 80 °C to remove the residual solvent, (ii) photoresist was spin coated onto the polystyrene film, exposed under UV irradiation for 12 s and then developed to pattern the source/drain electrode, (iii) the resulting sample was exposed again under UV irradiation for 12 s to enable the photoresist to dissolve in developer, (iv) deposited gold film with thickness of 20 nm, dislodged redundant photoresist with developer to obtain source/drain electrodes and finally deposited organic semiconductors of 50 nm pentacene to finish the fabrication of organic electronic devices. This “double exposure method” was also employed in the fabrication of logic circuit (inverter). The gate of the load transistor (T_L) was connected to its source to form “zero- V_{GS} load inverter”. The ratio of channel width/length (W/L) of the driving transistor (T_D) was larger (7 times) than those of the load transistor. The electrical characteristics of OFET devices were recorded at room temperature in air by using a Keithley 4200 SCS semiconductor parameter analyzer. The mobility of the devices was calculated in the saturation regime. The equation was listed as follows: $I_{DS} = (W/2L)C_i\mu(V_{GS} - V_{th})^2$, where W/L was the channel width/length, C_i was the insulator capacitance per unit area, and V_{GS} and V_{th} were the gate voltage and threshold voltage, respectively. X-ray photoelectron spectroscopy (XPS) and Atomic force microscope (AFM) were performed to characterize polystyrene films. Positive photo resist (RZJ-304) and the developer were purchased from Ruihong in China.

RESULTS AND DISCUSSION

The traditional and “double exposure method” process of photolithography was showed in Figure 1. In the traditional process of photolithography (route: (a) → (b) → (c) → (d) → (e)), the detailed procedure was as follows: (1) after one step exposure under UV irradiation, the exposed photoresist could dissolve in the developer whereas the unexposed area remained intact in the developer; (2) after one-step developing and metal

evaporation, redundant photoresist would be washed away by acetone to define the source/drain electrodes, called lift off. In lift-off process, conventional organic insulating materials were easily damaged or even dissolved (Figure 1e), and this was the reason why common organic insulators such as polystyrene (PS) were not selected as the dielectric layer materials in the previous report of photolithography. In our approach, a novel process called “double exposure method” (Figure 1, route: (a) → (b) → (c) → (f) → (g) → (h) → (i)) was utilized to define the source/drain electrodes with two-step exposure (Figure 1c, f), namely, after one time of exposure and developing, the remaining photoresist was exposed under UV irradiation again and then it was capable of dissolving in the developer, eliminating the usage of acetone to develop in the final lift-off step (Figure 1h), which avoided the damage to PS dielectric layers. Here, the main composition of the developer was tetramethyl ammonium hydroxide (TMAH, 2.38%), and the solvent was water; hence, PS layers could not dissolve in aqueous developer.

Atomic force microscope (AFM) images of spin-coated polystyrene (PS) films before and after photolithography process were shown in Figure 2. It clearly showed that the PS film surfaces were very smooth with root-mean-square (RMS) roughness at around 0.5 nm. The RMS roughness of film was slightly increased to 1.1 nm after photolithographic process, probably due to the solution effect during photolithographic processes. To validate whether the PS film was damaged during the “double exposure” processes, we performed X-ray photoelectron spectroscopy (XPS). As shown in Figure 3a, the typical peak of C_{1s} for PS film before and after photolithographic process was nearly identical, indicating the high stability of PS films against the developer and the integrity of chemical bond. In order to confirm the dielectric performance, the dielectric characteristics of PS dielectric films were evaluated via quantitative leakage current. Figure 3b showed the typical current density–voltage (J – V) plots of metal–insulator–metal structure fabricated with PS insulator, and low current density of about 1×10^{-7} to 1×10^{-9} A cm^{-2} was detected, demonstrating that the PS film undergone photolithography exhibited enough

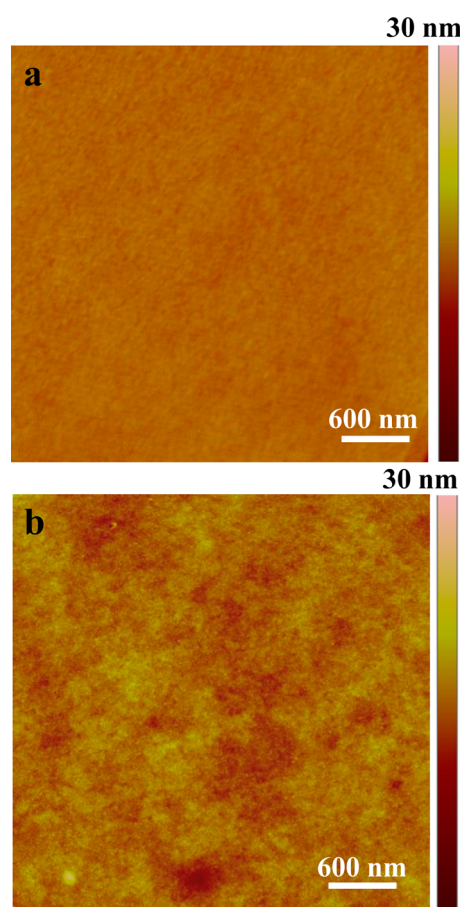


Figure 2. (a) AFM image of PS films before photolithography, (b) AFM image of PS films after photolithography.

good insulating properties for fabrication of organic electronic devices.

Furthermore, with “double exposure” process, the electrode arrays with channel length of 20 and 5 μm were successfully achieved (as shown in Figure 4). With these electrodes, bottom-gate bottom-contact (BGBC) OFETs with pentacene as semiconducting layers were fabricated on the flexible PET substrates (Figure 5a). Representative transfer and output characteristics of the transistors were shown in Figure 5b, c. The transistors exhibited excellent performance, which further indicated good electrical insulating property and good quality of the PS after “double exposure” process. The distribution of field-effect mobility of 100 devices was about $(0.2\text{--}0.36)\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, comparable to the BGBC OFETs with PS dielectric layers fabricated by shadow mask method $(0.3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1})$, and all these results were better than other early experimental results of BGBC OFETs with gold source/drain electrodes.²¹ After bending the flexible devices for 500 times over a 4 mm bending radius, the performance showed negligible change (see Figure S1 in the Supporting Information), implying the good prospect of this method in flexible electronics.

More significantly, “double exposure method” was extended to employ on other insulator materials, such as polymethyl methacrylate (PMMA). The PMMA film did not dissolve in developer after lift-off either. The OFETs based on PMMA dielectric layers also showed good performance with mobility reached $0.1\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ (see Figure S2 in the Supporting Information). The results

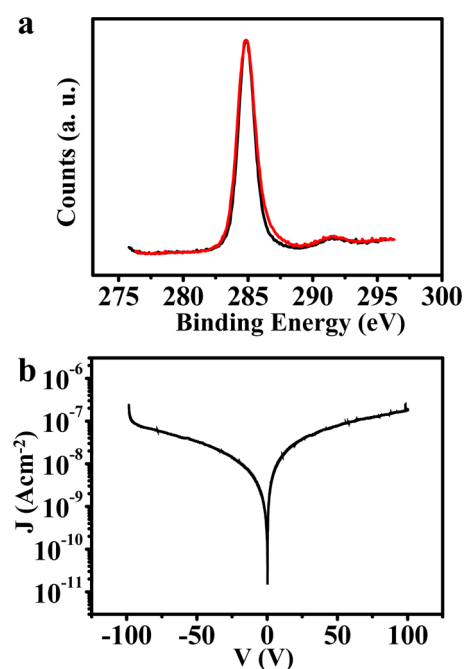


Figure 3. (a) XPS data of $\text{C}1\text{s}$ of the polystyrene before (black) and after (red) photolithography, and the XPS spectra are normalized in counts, (b) Typical current density–voltage (J – V) plots of metal–insulator–metal structure fabricated with PS insulator after photolithography.

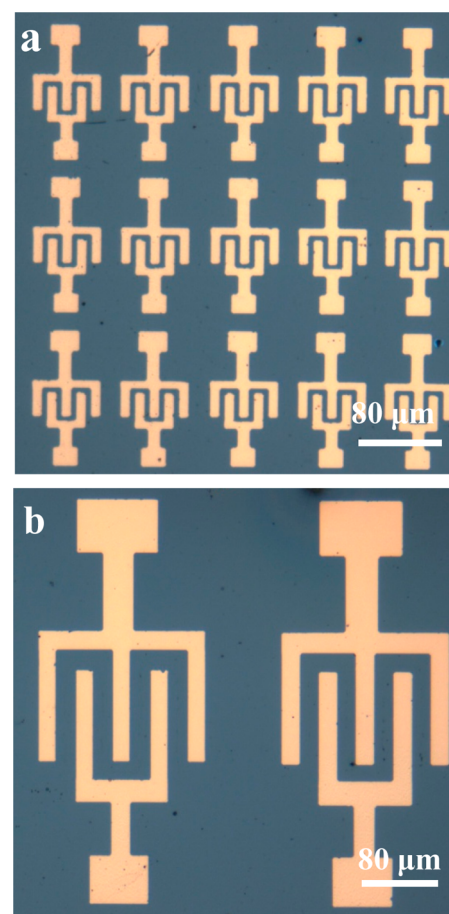


Figure 4. Different spacings of the electrode arrays fabricated through the “double exposure method”: (a) 5 μm and (b) 20 μm .

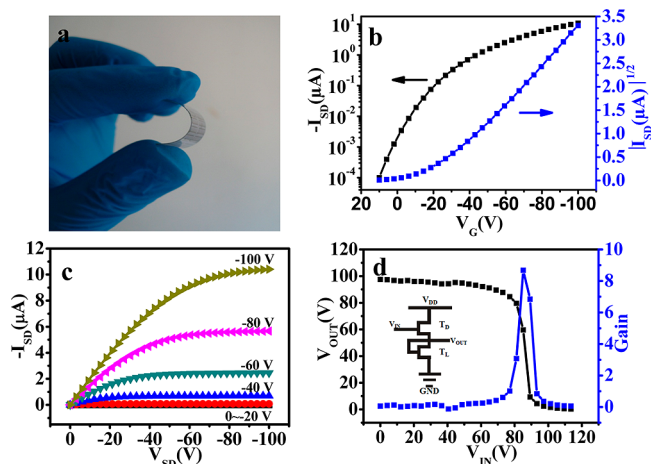


Figure 5. (a) Flexible OFETs and inverters fabricated on the PET substrate through the “double exposure method”, (b, c) Typical transfer and output characteristics of the transistor, (d) electrical characteristics of the organic inverters (the inset is the structure of organic inverter).

demonstrated this “double exposure method” was versatile to other common organic insulators.

Further, by adopting “double exposure” processes, we investigated the performance of logic circuits based on PS insulator and pentacene semiconductor. The transfer characteristics of a unipolar inverter based on pentacene were presented in Figure 5d. For low V_{in} , the V_{GS} of the driving transistor was negative, then the hole-conducting channel presented, and the resistance of the driving transistor was much smaller than that of the load transistor. Hence, the output voltage was close to V_{DD} . When V_{in} was high, V_{GS} of the driving transistor was close to zero. Then the output voltage was decided by the proportion of the W/L between the load transistor and the driving transistor. An inverter switch response was clearly observed from logic “0” to logic “1”, and the highest gain of 9 was obtained with the supply voltage of about 100 V.

CONCLUSION

In summary, a novel photolithographic process called “double exposure method” is introduced to fabricate flexible organic field-effect transistors and circuits. This method for the first time enables low-annealing-temperature polystyrene as an insulator layer in the process of photolithography. Besides, this “double exposure method” is versatile to other common organic insulators. High performance of transistors and circuits on the flexible substrates are achieved, which provides a new idea for the fabrication of flexible organic OFETs and circuits with high integration.

ASSOCIATED CONTENT

Supporting Information

Plots of mobility versus bending times on PET substrate based on PS insulator. Output and transfer curves for the OFET based on PMMA insulator. This material is available free of charge via the Internet at <http://pubs.acs.org>.

AUTHOR INFORMATION

Corresponding Author

*E-mail: huwp@iccas.ac.cn; ljiang@iccas.ac.cn.

Notes

The authors declare no competing financial interest.

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